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This document contains the supplementary information related to Electronics II Laboratory course for 2018-2019 fall semester of Electrical and Electronics Engineering curricula.

EEM 303 Electronics II Laboratory - JFET Summary

There are two principle types of transistors: bipolar junction transistors (BJTs), and field-effect transistors (FETs). The physical mechanisms underlying the operation of these two types of transistors are quite different. FETs are subdivided into two major classes: junction field-effect transistors (JFETs) and metal-oxide-semiconductor field-effect transistors (MOSFETs). Each type of FET is further subdivided into n-channel and p-channel FETs, and, for MOSFETs, enhancement and depletion MOSFETs.

JFETs has three terminals, a *voltage* on the gate terminal is used to control a *current* between two other terminals named the source and the drain. Gate voltage is referenced to the Source. Thus, V_{GS} refers to the voltage between the gate and the source, V_{DS} is the voltage between the drain and the source, I_D is the current into the drain, and I_S is the current out of the source. Under normal operating conditions**,** *no current flows into the gate***.** Consequently, $I_S = I_D$.

The JFET is a voltage-controlled device and which represents the rate of change of the Drain current with respect to the change in Gate-Source voltage. On the contrary, the BJT is a current-controlled device which can be easily seen with $I_C = \beta I_B$ equality.

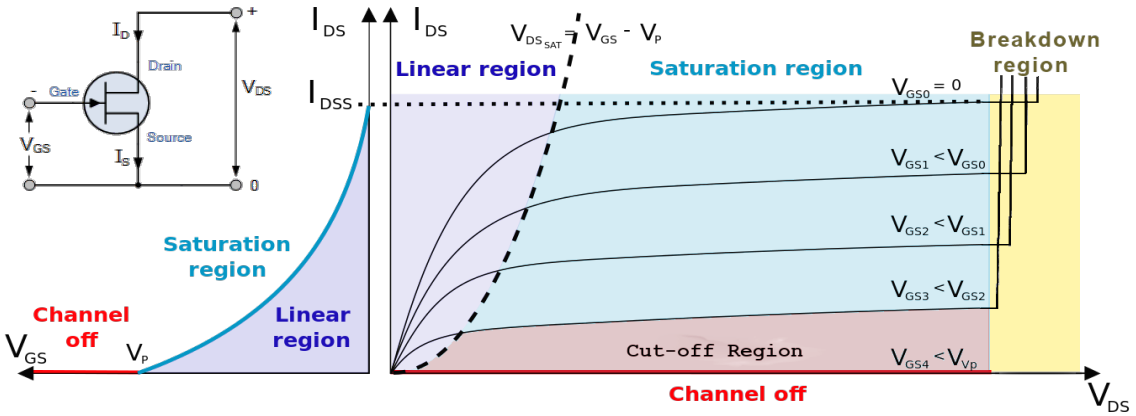


Figure 1: Input (left curve) and output (right curves) characteristics for n-channel JFETs. It is also called I-V characteristics

JFET is *saturated* when $V_{GS} = 0V$,
JFET is in *cut-off region* (also called *channel off*) when $V_{GS} < V_P$,
JFET is in *Linear region (Ohmic) when* $V_{GS} \geq V_P$

n-CHANNEL JFET

For all regions,

$$i_G = 0 \quad \text{for} \quad v_{GS} \le 0$$

Cutoff region:

$$i_D = 0 \quad \text{for} \quad v_{GS} \le V_P \quad (V_P < 0)$$

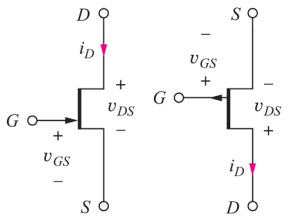
Linear (Triode or Ohmic) region:

$$i_D = \frac{2I_{DSS}}{V_P^2}\left(v_{GS} - V_P - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for} \quad v_{GS} \ge V_P \quad \text{and} \quad v_{GS} - V_P \ge v_{DS} \ge 0$$

Saturation (Active or Constant-current) region:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \quad \text{for} \quad v_{DS} \ge v_{GS} - V_P \ge 0$$

JFET circuit symbols.



(a) *n*-channel (b) *p*-channel

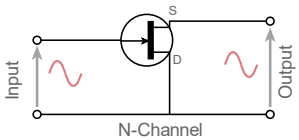
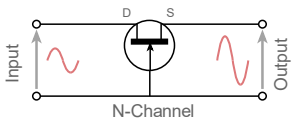
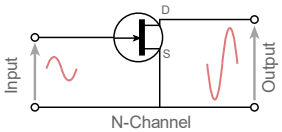
In the active region of JFET and in the formula of drain current I_D, where the I_{DSS} current is *the maximum possible current* with V_{GS} held at 0 V and the V_P voltage called pinch-off voltage. Pinch off voltage is the drain to source voltage (V_{DS}) after which the drain to source current (I_{DS} or I_D) becomes almost constant, and then JFET enters into saturation region that is defined only when gate to source voltage (V_{GS}) is zero. On the other hand, transconductance (g_m) is an expression of the performance of a bipolar transistor or field-effect transistor. The performance of the transistor is usually shown with a transconductance curve where I_D sketched versus V_{GS}. It can be defined as,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \ [S]$$

where g_m is the "transconductance gain" and the unit of g_m is called 'Siemens' which stand for 'S'

JFET is a majority charge carrier device hence it has less noise. Also, it is a low power consumption device which has high input impedance (~100MΩ). The JFETs occupies less space in circuits due to its smaller size. It is relatively more immune to radiation. Moreover, JFETs has negative temperature coefficient of resistance, so they possess higher Temperature Stability. As a disadvantage, the performance of JFET go downs as frequency increases due to feedback by internal capacitance.

Table 1: Summary of different configurated JFET characteristics

	 COMMON DRAIN, SOURCE FOLLOWER AMPLIFIER	 COMMON GATE TRANSISTOR AMPLIFIER	 COMMON SOURCE TRANSISTOR AMPLIFIER
Voltage gain	Zero	High	Medium
Current gain	High	Low	Medium
Power gain	Medium	Low	High
Input resistance	Very High	Low	Medium**
Output resistance	Low	High	Medium
Input / output phase relationship	0°	0°	180°

** Note: the input resistance for a FET itself is very high in view of the fact that it takes virtually no current

EEM 303 Electronics II Laboratory - MOSFET Summary

The metal-oxide-semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET) is a type of field-effect transistor (FET), most commonly fabricated by the controlled oxidation of silicon. It has an insulated gate; whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals. A metal-insulator-semiconductor field-effect transistor or MISFET is a term almost synonymous with MOSFET. Another synonym is IGFET for insulated-gate field-effect transistor.

The IGFET or MOSFET is a voltage-controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

This ultra-thin insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the MOSFET extremely high way up in the Mega-ohms (MΩ) region thereby making it almost infinite.

As the Gate terminal is electrically isolated from the main current carrying channel between the drain and source, *"NO current flows into the gate"* and just like the JFET, the MOSFET also acts like a voltage-controlled resistor where the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also, like the JFET, the MOSFETs very high input resistance can easily accumulate large amounts of static charge resulting in the MOSFET becoming easily damaged unless carefully handled or protected.

Like in the JFET experiment, MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The MOSFETs are available in two basic forms:

- *Depletion Type:* the transistor requires the Gate-Source voltage, (VGS) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.
- *Enhancement Type:* the transistor requires a Gate-Source voltage, (VGS) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

The symbols and basic construction for both configurations of MOSFETs are shown in Figure 2.

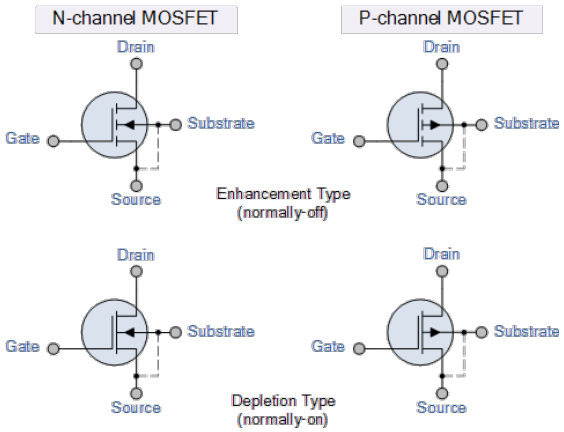
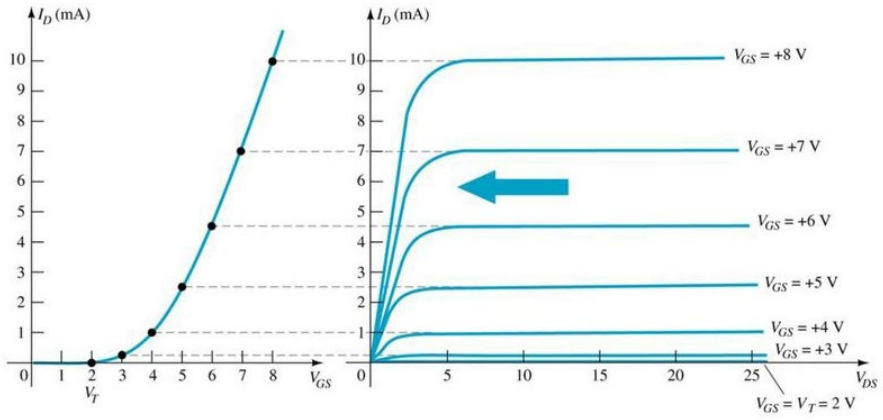


Figure 2: Frequency curve response

Some MOSFETs are used as drive amplifiers, especially in high power controls. Hence, this type of transistors is called Power MOSFETs which have wider channel structure. The structure is vertical and not planar. Using a vertical structure, it is possible for the transistor to sustain both high blocking voltage and high current. This type of Power MOSFETs is called Vertical MOSFETs, also shortly V-MOSFETs.

The Enhancement mode MOSFET only operates in the enhancement mode.



V_{GS} is always positive
I_{DSS} = 0 when V_{GS} < V_T
As V_{GS} increases above V_T, I_D increases
If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})
The saturation level, V_{DSsat} is reached.

The behavior of a MOSFET transistor in depletion and enhancement modes depending on the gate voltage is summarized as follows.

MOSFET TYPE	V_{GS} = +VE	V_{GS} = 0	V_{GS} = -VE
N-channel Depletion	ON	ON	OFF
N-channel Enhancement	ON	OFF	OFF
P-channel Depletion	OFF	ON	ON
P-channel Enhancement	OFF	OFF	ON

Frequency Response of an electric or electronics circuit allows us to see exactly how the output gain (known as the magnitude response) and the phase (known as the phase response) changes at a particular single frequency, or over a whole range of different frequencies from 0Hz, (DC) to many thousands of mega-hertz, (MHz) depending upon the design characteristics of the circuit. Generally, the frequency response analysis of a circuit or system is shown by plotting its gain, that is the size of its output signal to its input signal, Output/Input against a frequency scale over which the circuit or system is expected to operate. Then by knowing the circuits gain, (or loss) at each frequency point helps us to understand how well (or badly) the circuit can distinguish between signals of different frequencies.

In Electronics, the Logarithm, or "log" for short is defined as the power to which the base number must be raised to get that number. Then on a Bode plot, the logarithmic x-axis scale is graduated in $\log_{10}$ divisions, so every decade of frequency (e.g, 0.01, 0.1, 1, 10, 100, 1000, etc.) is equally spaced onto the x-axis. The opposite of the logarithm is the antilogarithm or "antilog".

Graphical representations of frequency response curves are called **Bode Plots** and as such Bode plots are generally said to be a semi-logarithmic graph because one scale (x-axis) is logarithmic and the other (y-axis) is linear (log-lin plot) as shown.

Frequency Response Curve

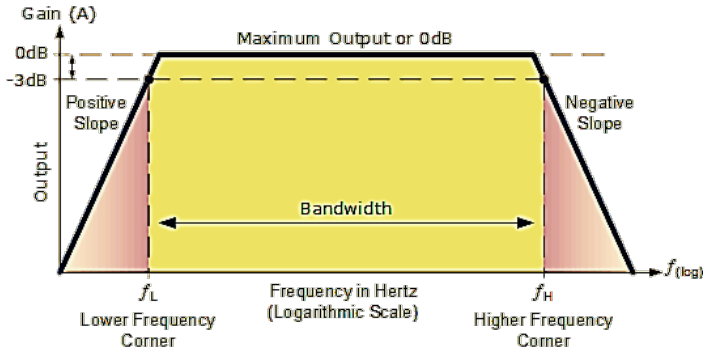


Figure 3: Frequency curve response

Frequency points f_L and f_H relate to the lower corner or cut-off frequency and the upper corner or cut-off frequency points respectively were the circuits gain falls off at high and low frequencies. These points on a frequency response curve are known commonly as the -3dB (decibel) points. So, the bandwidth is simply given as:

$$Bandwitdh = BW = f_H - f_L$$

Although there are several choices to define *Bandwidth* interval, the -3dB points are chosen as the bandwidth limits. The -3dB point is also known as the *half-power* points since the output power at this corner frequencies will be half that of its maximum 0dB value as shown in the Figure 3.

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