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Faculty of Engineering
Electrical and Electronics Engineering

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EEM 303 Electronic II Laboratory 5

Source Grounded JFETs

	Student Name	Student ID	Group Number
1.			
2.			
3.			
4.			

Objective:

To observe and understand terminally grounded JFETs

Equipment will be available at the laboratory:

DC power supply, Oscilloscope, Electronic Training Set(Y-0016), Patch wires,

Equipment will be ensured by students:

Digital Multi-Meter

Preliminary Work:

Read the laboratory sheets. There might be a test or classical exams in the beginning of each laboratory hour. Questions will be asked mostly from *Supplementary Information* and *Procedure* sections.

Compare the Drain, Gate and Source grounded JFETs, in terms of;

- Voltage Gain (A_V),
- Current Gain (A_I),
- Power Gain, (A_P),
- Input Resistance, (R_{in}),
- Output Resistance, (R_{out}),
- Phase Shift (θ)

and document it into A4 paper. Preliminary works should be given to instructor(s) at beginning of laboratory hour.

Procedure:

1. Turn on the oscilloscope and calibrate it,
2. Make sure the amplitude and frequency potentiometer of Function Generator adjusted to minimum, then, turn on the Training Set and connect the 'OUTPUT' to first channel of the oscilloscope,
3. Adjust the frequency to 1kHz and peak to peak voltage ($V_{i_{pp}}$) to $100\ mV$
4. Power off the Training Set and Oscilloscope,
5. Insert the Y-0016-0011 module into training set.
6. Connect the patch wires to the module as it is shown in Figure 1.
7. Turn the power on for Y-0016 Training Set.

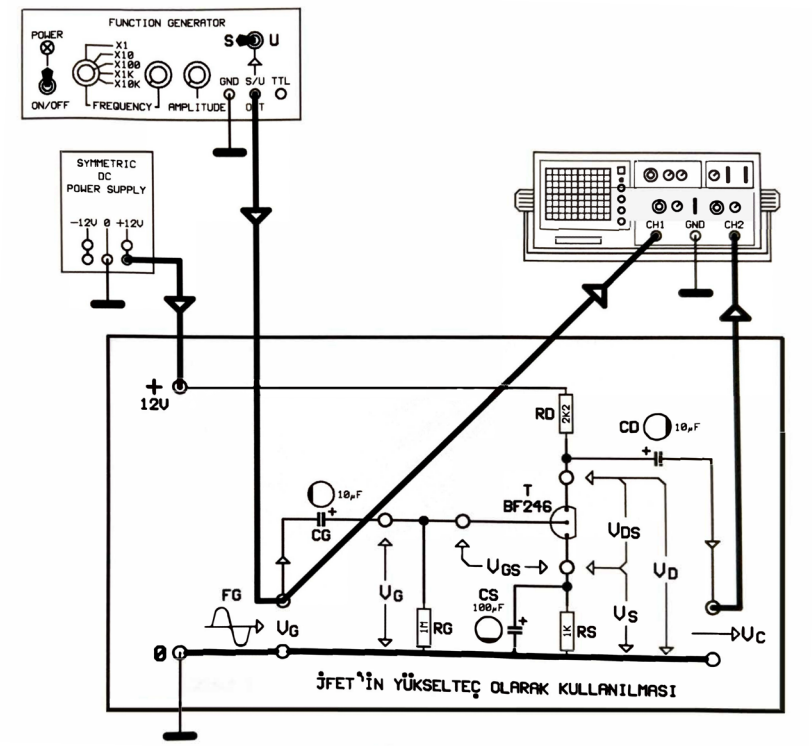

Figure 1: Connection scheme of source grounded JFET

8. Make sure the Function Generator is off, then measure the terminal voltages; V_G, V_{GS}, V_S, V_{DS} and V_D and fill the Table 1 with measured values.
9. Turn the Function Generator on and sketch the input and output signal into Figure 2.
10. Calculate the Voltage Gain (A_V) and measure the Phase Shift θ,

During the experiment, JFET increases its resistance by increasing the drain current. As a result, the drain current begins to decrease. The resulting heat can also damage the JFET. Therefore, values should be taken as quickly as possible in measurement steps!

Results:

Table 1: Voltage measurements of the JFET terminals and the voltage drop between the terminals

V_G	V_{GS}	V_S	V_{DS}	V_D

Input Signal
Volt/div = …….
Time/div = …….

Output Signal
Volt/div = …….
Time/div = …….

Voltage Gain
$A_V =$

Phase Shift

$\theta =$

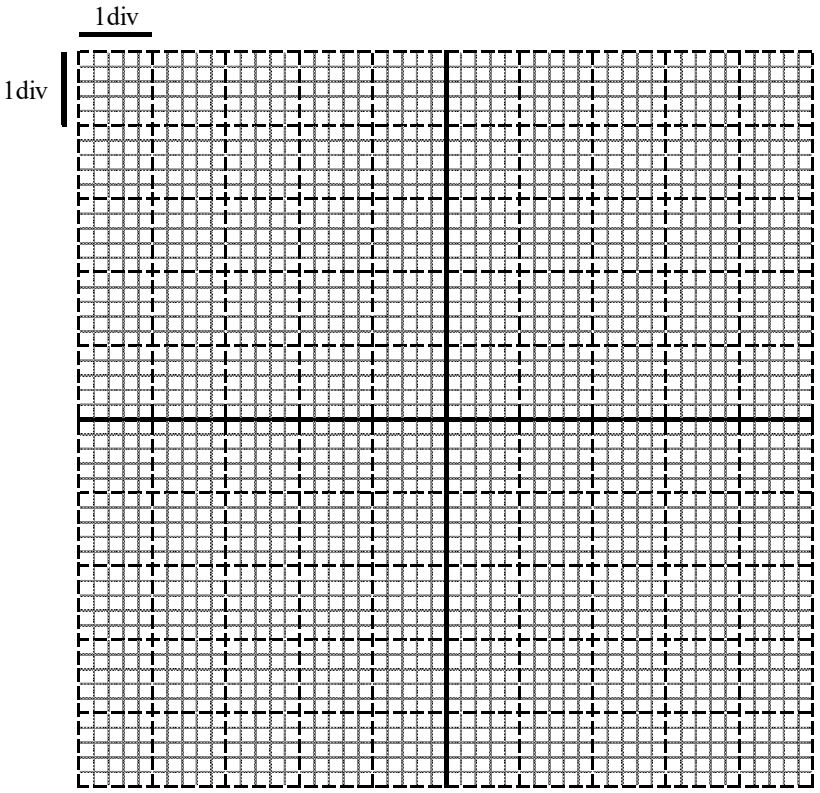

Figure 2: Input signal versus output signal oscillograph for source grounded JFET

Conclusion: